

Characterization of Regulated Converters to Ensure Stability and Performance in Distributed Power Supply Systems

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Abstract

The characterization of regulated converters is investigated in order to establish a set of dynamical parameters defining the interactions arising in the interconnected systems such as telecom distributed power supply (DPS) systems. The commercially available converters are usually vaguely specified in respect to those interactions. Provided information do not suffice for predicting the stability and performance. It is noticed that there are certain double reflections, which are not previously recognized but may increase the load sensitivity if not properly considered. The defined parameter set can be also used to design the converters to be more insensitive to different interactions.

1 Introduction

Telecom power supply systems are regularly based on the use of distributed architectures (DPA, DPS), where regulated converters are supplying other regulated converters [1]-[4] as illustrated in Fig. 1. The regulated converters are prone to interactions from the supply and load sides [5]-[15]. Basically it is a question of different impedances of the converter and the system, which would affect the internal dynamics of a converter. The input impedance of the regulated converter may behave as a negative resistor [5],[6] and drive even a passive LC circuit into instability (i.e., negative resistor oscillation).

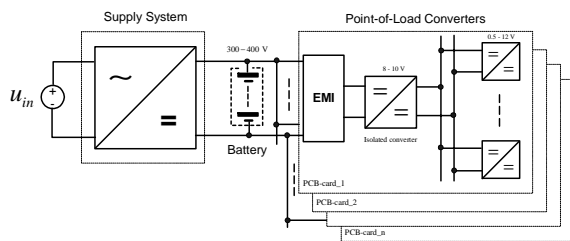


Fig. 1 Typical DPS system in telecom applications

The formalism to solve the input side interactions were basically developed in early 1970 [5],[6] utilizing the canonical equivalent circuit [7] valid only for continuous conduction mode (CCM) and direct-duty-ratio or voltage-mode control. The limited direct applicability of the equations behind the formalism has hindered the full understanding of the phenomena behind the interactions. The more general equations developed in [14],[15] solved the problem of understanding even if it is otherwise claimed in [12].

The output or load side interactions have been studied intensively since mid 1985 [8]-[11] utilizing actually the formalism developed in [5],[6]. It is well known that an impedance-type load can affect the dynamics of a converter and cause even instability [8]-[10]. It is claimed that the load interactions can be cancelled designing the closed-loop output impedance to be small [[10],[11]. The load interactions are, however, propagated into the converter dynamics through the open-loop output impedance [19], and consequently, the small closed-loop output impedance does not necessarily guarantee load invariance for arbitrary load.

Even if the different interaction mechanisms have been discussed and analyzed for tens of years, the commercially available converters as e.g. [16],[17] are not usually specified in a manner providing sufficient information for predicting system level stability and performance. The goal of the paper is to provide such a set of dynamical parameters, which are sufficient for performing the required analyses. The proper interaction formalism is derived using the methods based on the unterminated two-port modelling technique described in [19]. The extra element theorem [18],[20] can be also used for extracting the parameters but its complexity favours the use of the two-port modelling technique, when the whole set of the parameters has to be defined.

The rest of the paper is organized as follows: The interaction formalism and the describing equations are derived and discussed in Section 2. The measurement of the defined parameters is discussed and experimental data are provided based on a VMC buck converter in Section 3. The conclusions are presented in Section 4.

2 Interaction Formalism

The dynamics associated to a switched-mode converter is typically represented using a set of transfer functions (1) known as G -parameters defining also a linear two-port circuit [19] shown in Fig. 2 inside the dashed line. The input port of the model is a *Norton* equivalent circuit, and the output port a *Thevenin* equivalent circuit. The first row of the matrix in (1) defines the input port and the second row defines the output port, respectively. The negative sign of the output impedance is a consequence of the direction of the output current sink, and has to be omitted, when picking the parameters. Both of the representations are given in an unterminated mode, i.e., the load effect is excluded and therefore, the set describes the internal dynamics of the converter. The general control variable in (1) is denoted by \hat{c} .

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \end{bmatrix} = \begin{bmatrix} Y_{in-o}^* & T_{ji-o}^* & G_{ci}^* \\ G_{io-o}^* & -Z_{o-o}^* & G_{co}^* \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{i}_o \\ \hat{c} \end{bmatrix} \quad (1)$$

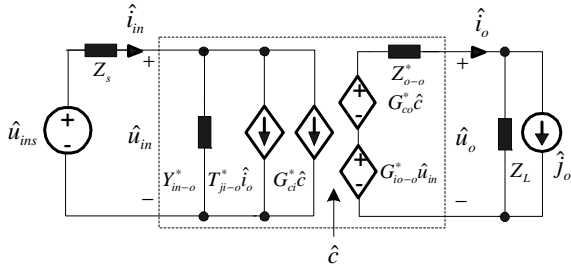


Fig. 2 Unterminated two-port model (inside the dashed line) and an impedance-type source and load.

2.1 Load Interactions

The effect of the impedance-type load on the converter dynamics can be found computing \hat{u}_o and \hat{i}_o from the output port (Fig. 2) at the presence of the load, which gives (2). The equation for \hat{u}_o in (2) defines explicitly the load-affected output dynamics. The load-affected input dynamics can be found replacing \hat{i}_o in the input port with the equation of \hat{i}_o in (2). The corresponding load-affected transfer-function matrix is shown in (3).

$$\begin{aligned} \hat{u}_o &= \frac{G_{io-o}^* \cdot \hat{u}_{in} - Z_{o-o}^* \cdot \hat{j}_o + G_{co}^* \cdot \hat{c}}{1 + \frac{Z_{o-o}^*}{Z_L}} \\ \hat{i}_o &= \frac{G_{io-o}^* \cdot \hat{u}_{in} + Z_L \cdot \hat{j}_o + G_{co}^* \cdot \hat{c}}{Z_L + Z_{o-o}^*} \end{aligned} \quad (2)$$

$$\begin{bmatrix} Y_{in-o}^* + \frac{G_{io-o}^* T_{ji-o}^*}{Z_L + Z_{o-o}^*} & \frac{Z_L T_{ji-o}^*}{Z_L + Z_{o-o}^*} & G_{ci}^* + \frac{G_{co}^* T_{ji-o}^*}{Z_L + Z_{o-o}^*} \\ \frac{G_{io-o}^*}{1 + \frac{Z_{o-o}^*}{Z_L}} & -\frac{Z_{o-o}^*}{1 + \frac{Z_{o-o}^*}{Z_L}} & \frac{G_{co}^*}{1 + \frac{Z_{o-o}^*}{Z_L}} \end{bmatrix} \quad (3)$$

2.2 Source Interactions

The effect of the impedance-type source on the converter dynamics can be found computing \hat{u}_{in} and \hat{i}_{in} in the input port (Fig. 2) at the presence of the source impedance Z_s , which gives (4). The corresponding source-affected transfer-function matrix is shown in (5). Y_{in-sc} and $Y_{in-\infty}$ of (5) are defined in (6), respectively.

$$\begin{aligned} \hat{u}_{in} &= \frac{\hat{u}_{ins} - Z_s T_{ji-o}^* \cdot \hat{i}_o - Z_s G_{ci}^* \cdot \hat{c}}{1 + Z_s Y_{in-o}^*} \\ \hat{i}_{in} &= \frac{Y_{in-o}^* \cdot \hat{u}_{ins} + T_{ji-o}^* \cdot \hat{i}_o + G_{ci}^* \cdot \hat{c}}{1 + Z_s Y_{in-o}^*} \end{aligned} \quad (4)$$

$$\begin{bmatrix} \frac{Y_{in-o}^*}{1 + Z_s Y_{in-o}^*} & \frac{T_{ji-o}^*}{1 + Z_s Y_{in-o}^*} & \frac{G_{ci}^*}{1 + Z_s Y_{in-o}^*} \\ \frac{G_{io-o}^*}{1 + Z_s Y_{in-o}^*} & -\frac{1 + Z_s \cdot Y_{in-sc}}{1 + Z_s Y_{in-o}^*} \cdot Z_{o-o}^* & \frac{1 + Z_s \cdot Y_{in-\infty}}{1 + Z_s Y_{in-o}^*} \cdot G_{co}^* \end{bmatrix} \quad (5)$$

$$\begin{aligned} Y_{in-sc} &= Y_{in-o}^* + \frac{G_{io-o}^* T_{ji-o}^*}{Z_{o-o}^*} \\ Y_{in-\infty} &= Y_{in-o}^* - \frac{G_{io-o}^* G_{ci}^*}{G_{co}^*} \end{aligned} \quad (6)$$

2.3 Interaction Parameters

The transfer function matrix in (1) describes fully the internal dynamics of a converter, which may be evoked by using an ideal source voltage (i.e., $Z_s = 0$) and loading the converter with a constant-current sink (i.e., $Z_L = \infty$) [19]. The stability and robust performance of a converter can be studied by means of the loop gain associated to the controlled output variable. According to the closed-loop control-block diagram shown in Fig. 3, we can compute the output-voltage loop gain $L(s)$ to be as shown in (7). It is obvious that the changes in the control-to-output transfer function G_{co} would reflect also changes in the loop gain.

$$L(s) = H_v G_{cc} G_{ca} G_{co} \quad (7)$$

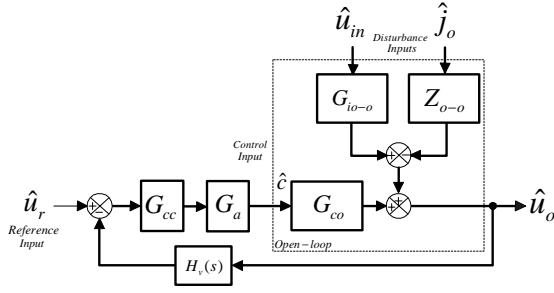


Fig. 3 Control-block diagram for closed-loop output dynamics.

According to (3), the load interactions would affect the loop gain as defined in (8), where $L^*(s)$ denotes the internal loop gain. The open-loop internal output impedance Z_{o-o}^* plays a decisive role in the load interactions.

$$L(s) = \frac{L^*(s)}{1 + \frac{Z_{o-o}^*}{Z_L}} \quad (8)$$

According to (5), the source interactions would affect the loop gain as defined in (9). In the source interactions, there are two circuit elements in addition with the source impedance Z_s having effect on the interactions - namely the load-dependent open-loop input admittance Y_{in-o} and the closed-loop input admittance with infinite bandwidth controller $Y_{in-\infty}$ [19],[20]. It may be obvious that $Y_{in-\infty}$ is a special circuit element: It has been shown in [14],[15] that $Y_{in-\infty}$ is independent of load and even control mode for a given converter. Therefore, it can be computed as defined in (10), where the subscript extension ‘-v’ stands for voltage-mode control.

$$L(s) = \frac{1 + Z_s Y_{in-\infty}^*}{1 + Z_s Y_{in-o}^*} \cdot L^*(s) \quad (9)$$

$$Y_{in-\infty} = Y_{in-\infty}^* = Y_{in-o-v}^* - \frac{G_{io-o-v}^* G_{ci-v}^*}{G_{co-v}^*} \quad (10)$$

If we look more carefully the source effects in (5), we notice that the source impedance may change also the internal open-loop output impedance. As a consequence, the load sensitivity may be increased. Therefore, the double-affected loop gain can be presented as shown in (11). According to [20], Y_{in-sc} is the open-loop input admittance, when the load is a short circuit. This means that Y_{in-sc} is independent of load but dependent on topology and control mode as defined in (6).

$$L(s) = \frac{(1 + Z_s Y_{in-\infty}^*)}{1 + Z_s Y_{in-o}^* + \frac{(1 + Z_s Y_{in-sc}^*) Z_{o-o}^*}{Z_L}} \cdot L^*(s) \quad (11)$$

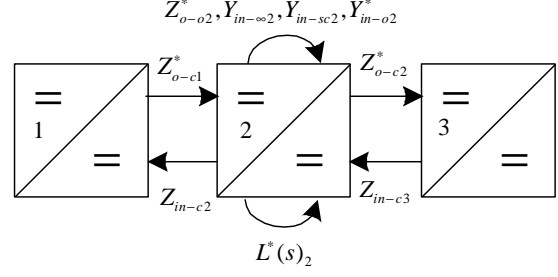


Fig. 4 Set of parameters for computing the load and source interactions in a regulated converter.

The set of parameters by means of which the source and load interactions in a regulated converter can be predicted using computational methods, is defined in Fig. 4. The straight lines with arrow ends define the parameters needed from the other system elements (i.e., from the elements 1 and 3 for 2) for carrying out the analysis. The curved lines define the internal parameters within an associated converter. If it is desired to analyze all the dynamical properties involved in a regulated converter, the whole set of open-loop transfer functions (1) has to be given naturally at the operating point most critical to the converter dynamics.

The internal stability of a system can be inferred using four special transfer functions [21] of which one is as specified in (12). If the system elements are of minimum-phase subsystems, the internal stability can be inferred using e.g. (12). If the subsystems are of non-minimum-phase elements, it may be necessary to study the stability of all the four transfer functions. The corresponding impedances in (12) are closed-loop impedances, and their ratio is ‘a main loop gain’ for which the *Nyquist* stability criteria can be applied. It must be emphasized that the performance figures (i.e., gain and phase margins) deduced using the closed-loop impedance ratio (i.e., $Z_{o-c(i)}^* / Z_{in-c(i+1)}^*$) do not necessarily comply with the performance figures of the corresponding supply or load-side converter.

$$\frac{1}{1 + \frac{Z_{o-c(i)}^*}{Z_{in-c(i+1)}^*}} \quad (12)$$

3 Experimental Measurements

The VMC buck converter specified in Fig. 5 was used as an example for the characterization. The frequency –response (FR) measurements are carried out using *Venable Industries*’ FR analyzer *Model 3120* with an impedance measurement set including the linear amplifier *Model VLA 1000* and an injection transformer. The data obtained from the FR analyzer were transformed to Matlab™ data form for efficient figure handling.

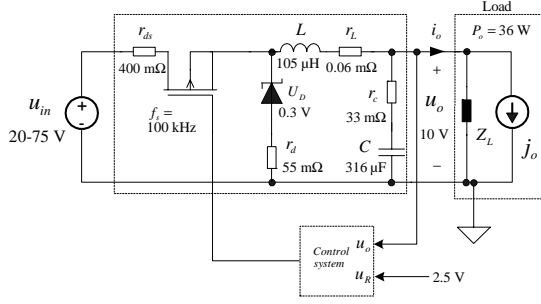


Fig. 5 Experimental VMC buck converter

The measurement of the open- and closed-loop basic transfer functions can be carried out easily. The dynamics of the FR analyzer (i.e., minimum ≈ -60 dB) set some limits for achieving correct measurements for the closed-loop input admittance and internal output impedance. The measurements were made by using a pure resistor of 4Ω as a load, and the load effect was removed computationally applying the information given in (3). It also turned out that a constant-current sink may not behave dynamically as assumed and can significantly affect the measured transfer functions. Therefore, it was deemed appropriate to use a pure resistor as a load and use computational methods to extract the unterminated transfer functions if necessary.

The direct measurement of the ideal input admittance $Y_{in-\infty}$ and the open-loop-short-circuit admittance Y_{in-sc} is impossible but can be computed from the frequency responses of the transfer functions specified in (6).

An attempt to predict the influence of the source impedance is presented in [12]. It is based on the observation that $Y_{in-\infty}$ is measurable by using the loop gain measurement, when the source impedance is very high. Consequently, the theoretical loop gain may be presented as shown in (13) according to (5). It is concluded that such a source is a constant-current source, which should be used to supply the converter during the measurement of the corresponding loop gain $L_\infty(s)$ (i.e., T_∞ in [12]). It may be obvious that such a measurement condition is practically impossible, and therefore, the validity of the obtained loop gain may be questionable.

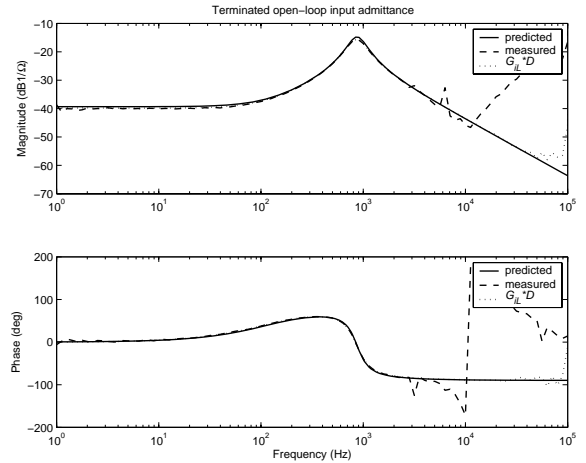
$$\lim_{Z_s \rightarrow \infty} L(s) = \frac{Y_{in-\infty}}{Y_{in-o}^*} L^*(s) \quad (13)$$

It is, however, possible to derive an equation by using closed-loop input admittance Y_{in-c} and a specific source impedance Z_{s1} to solve $Y_{in-\infty}$ as shown in (14), where $L^{Z_{s1}}(s)$ is the measured loop gain at the source impedance Z_{s1} . The loop gain for the arbitrary source impedance Z_s can be obtained replacing $Y_{in-\infty}$ in (9) with (14).

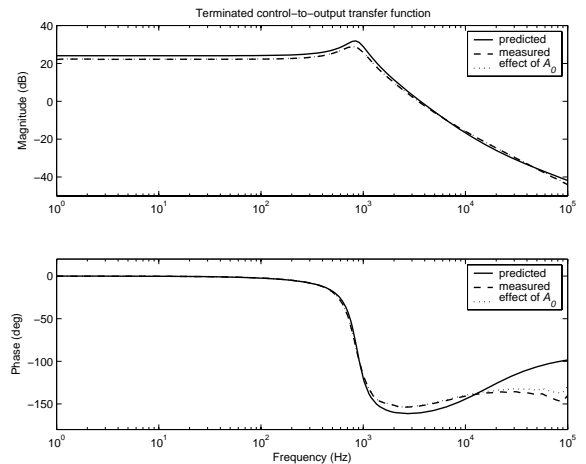
$$Y_{in-\infty} = \frac{L^{Z_{s1}}(s)}{1 + L^{Z_{s1}}(s)} \left[\frac{(1 + L^*(s))Y_{in-c}}{L^*(s)} - \frac{1}{Z_{s1}} \left(\frac{1}{L^{Z_{s1}}(s)} - \frac{1}{L^*(s)} \right) \right] \quad (14)$$

3.1 Ideal Input Admittance

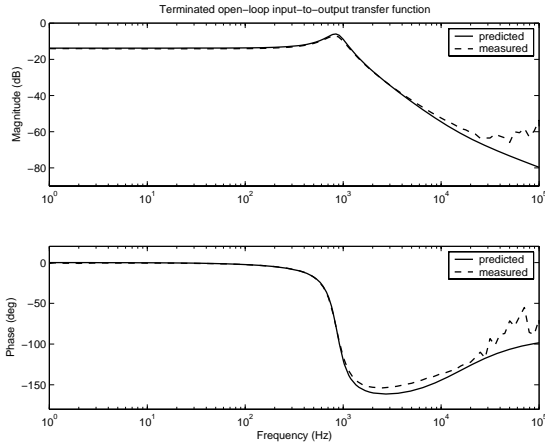
The ideal or infinite-bandwidth input admittance $Y_{in-\infty}$ can be computed to be equal to $-DI_L/U_{in}$ for the basic buck converter in CCM using (10) [19]. The open-loop transfer functions in (10) were measured at the input voltage of 50 V using a resistive load of 4Ω and are shown in Fig. 6. The dashed lines correspond to the measurements and the solid lines for the predictions. Several non-idealities were observed causing the measurements to deviate from the predictions. Their effect can be removed computationally if the phenomenon is known.



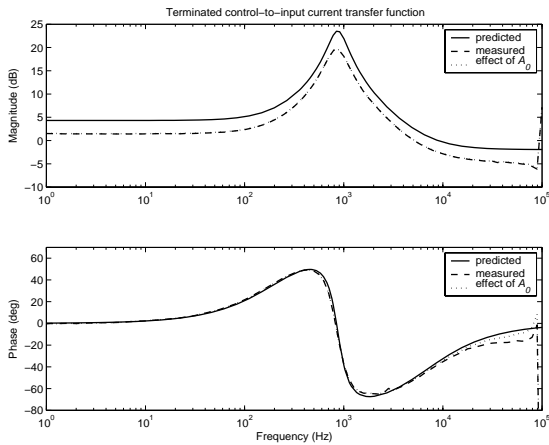
a) Open-loop input admittance Y_{in-o}



b) Control-to-output transfer function G_{co}



c) Input-to-output transfer function G_{io-o}



d) Control-to-input transfer function G_{ci}

Fig. 6 The measured (dashed lines) and predicted (solid lines) open-loop transfer functions defining $Y_{in-\infty}$

The predicted and computed $Y_{in-\infty}$ is shown in Fig. 7. The computation is based on the measured frequency-responses shown in Fig. 6. In principle, the compliance between the prediction and the measurement-based frequency responses is good but the uncertainties in the measured frequency responses (Fig. 6) will cause easily errors, which concentrate at the resonant frequency and higher frequencies as is visible in Fig. 7. The FR measurements, where the other variable is a pulsating current, are challenging. Even small stray inductances can cause undesired oscillations, and consequently, the deterioration of the measurement. The practical converters are typically equipped with input filters, and therefore, the accuracy of the measurement would be better.

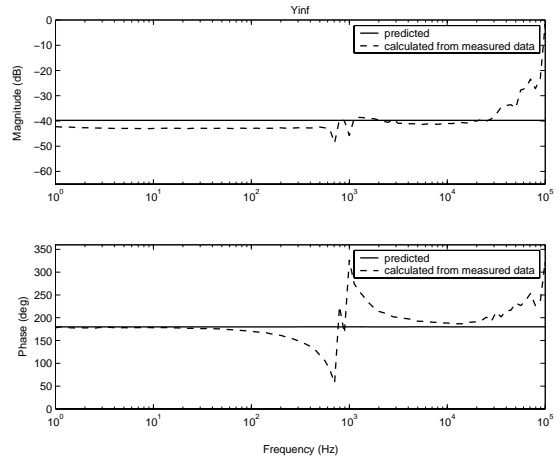


Fig. 7 Ideal input admittance $Y_{in-\infty}$

3.2 Short-Circuit Input Admittance

The short-circuit open-loop input admittance Y_{in-sc} can be computed to be for the basic buck converter (Fig. 5) according to (6) as shown in (14). Y_{in-sc} can be computed by using the frequency responses of the corresponding transfer functions as in the case of $Y_{in-\infty}$. Due to the space limitations, the measurements are not shown.

$$Y_{in-sc} = \frac{D^2}{r_L + Dr_{ds} + D'r_d + sL} \quad (15)$$

3.3 Loop Gain

The predicted and measured loop gain $L(s)$ of the converter is shown in Fig. 8. The mismatch between the prediction and measurement is due to a pole at 100 kHz in the used PWM modulator, which is not considered in the prediction. The same mismatch is observable in Fig. 6b (i.e., G_{co}).

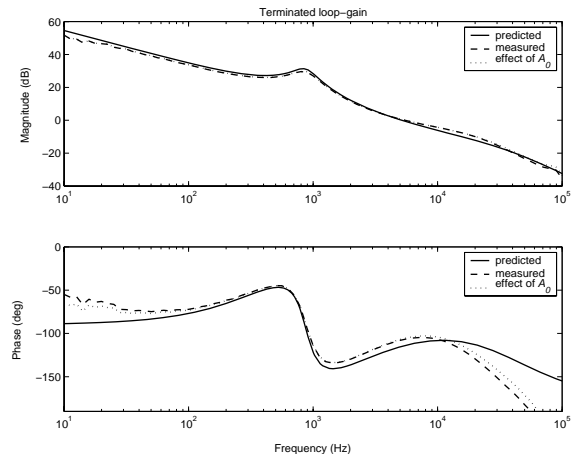


Fig. 8 The loop gain $L(s)$

The characterization of regulated converters in order to analyze and predict their dynamical behaviour in an interconnected system was investigated. A set of dynamical parameters describing those interactions was developed. It was observed that the dynamical information provided by the manufactures is not usually sufficient for assessing the stability and performance of the regulated converters and interconnected systems. The defined set consists of five explicit and two implicit parameters. The explicit parameters are the corresponding open- and closed-loop transfer functions and the internal loop gain. The implicit parameters – ideal input admittance and open-loop short-circuit admittance - have to be computed based on the measured frequency responses of the specified open-loop transfer functions. The defined set of the interaction parameters would give information on the methods to minimize the interactions as well.

6

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