Load-Impedance Based Interactions in Regulated Converters

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Abstract

The effect of load impedance on the dynamics and performance of a regulated converter is investigated. Theoretical formulation is derived utilizing two-port modelling technique. It is definitively shown that the load interactions are reflected into the converter dynamics via the internal open-loop output impedance. At the frequencies, where the loop gain is much higher than unity, the internal closed-loop output impedances acts as a boundary for the control-bandwidth reduction. The loop gain is always affected, whenever the internal open-loop output impedance is equal or greater than the load impedance. The converters are sensitive especially to the capacitive and resonant-type loads. The sensitivity is dependent on control mode, and cannot be much reduced by means of basic controller design.

1 Introduction

Telecom power supply systems are regularly based on the use of distributed architectures (DPA, DPS), where regulated converters are supplying other regulated converters [1]-[3] as illustrated in Fig. 1. In order to meet stringent international EMC requirements, the converters have to be equipped with EMI filters to suppress the noise at acceptable level. Extra capacitors have to be added sometimes at the output of the converter to improve the transient response. Both of these additional elements may significantly change the nature of the load seen by the supplying converter and can cause instability or deterioration of performance [4]-[7].

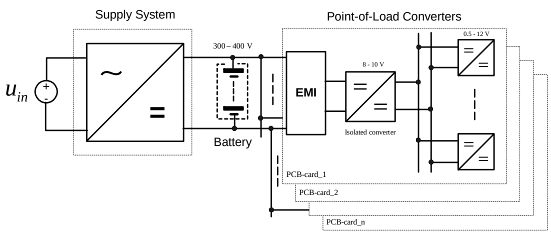

Fig. 1 Typical DPS system in telecom applications

The desire would be that the supplying converters can be designed to be insensitive to the variations in the load dynamics, i.e., load invariant similarly to the input invariance discussed in [8]. It is claimed that the load invariance can be achieved by designing the closed-loop internal output impedance of the supplying converter to be small [5]-[7]. The formalism defining the load effect on the converter can be obtained by utilizing either extra element theorem [9], unterminated two-port modelling [10],[11] or robust control method (i.e., star product) [14]. According to this formalism, the load interactions are reflected into the converter via the internal (i.e., unterminated) open-loop output impedance as shown in detail in Section 2 [10]. The closed-loop output impedance would act as a boundary for the control-bandwidth reduction at those frequencies, where the magnitude of the loop gain is much greater than unity. The phase of the loop gain is changed always, whenever the magnitude of the load impedance is close to or smaller than the unterminated open-loop output impedance. The paper will show that definitively. As a consequence, the real load invariance may be achieved only utilizing methods, which reduce the open-loop unterminated output impedance as discussed in [15].

The rest of the paper is organized as follows: The load-interaction formalism is derived and discussed in Section 2. Experimental evidence on load interactions is provided in Section 3 using a voltage-mode-controlled (VMC) buck converter as an example. The design of load invariance is shortly introduced in Section 4. The conclusions are presented in Section 5.

2 Load-Interaction Formalism

The dynamics associated to a switched-mode converter is typically represented using a set of transfer functions (1) known as *G*-parameters [12], which defines a linear two-port model [10] shown in Fig. 2. The input port of the model is a *Norton* equivalent circuit, and the output port a *Thevenin* equivalent circuit. The first row of the matrix in (1) defines the input port and the second row defines the output port, respectively. The negative sign of the output impedance is a consequence of the direction of the output current sink, and has to be omitted, when picking the parameters. Both of the representations are given in an unterminated mode, i.e., the load effect is excluded. The general control variable in (1) is denoted by $\hat{c}$.

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \end{bmatrix} = \begin{bmatrix} Y^*_{in-o} & T^*_{ji-o} & G^*_{ci} \\ G^*_{io-o} & -Z^*_{o-o} & G^*_{co} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{i}_o \\ \hat{c} \end{bmatrix} \tag{1}$$

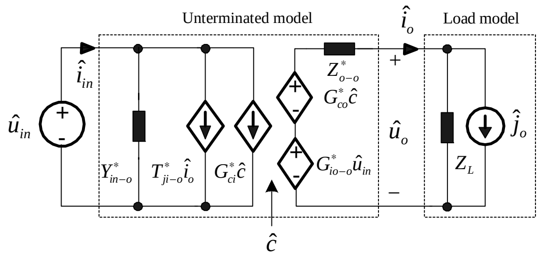

Fig. 2 Unterminated two-port model (inside the dashed line) and an impedance-type load.

The effect of the impedance-type load in the converter dynamics can be found computing $\hat{u}_o$ and $\hat{i}_o$ from the output port at the presence of the load, which gives (2). The equation for $\hat{u}_o$ in (2) defines explicitly the load-affected output dynamics. The load-affected input dynamics can be found replacing $\hat{i}_o$ in the input port with the equation of $\hat{i}_o$ in (2), which gives $\hat{i}_{in}$ shown in (3). The equation (3) defines explicitly the load-affected input dynamics, respectively.

$$\hat{u}_o = \frac{G^*_{io-o}\cdot\hat{u}_{in} - Z^*_{o-o}\cdot\hat{j}_o + G^*_{co}\cdot\hat{c}}{1+\dfrac{Z^*_{o-o}}{Z_L}}$$
$$\hat{i}_o = \frac{G^*_{io-o}\cdot\hat{u}_{in} + Z_L\cdot\hat{j}_o + G^*_{co}\cdot\hat{c}}{Z_L + Z^*_{o-o}} \tag{2}$$

$$\hat{i}_{in} = (Y^*_{in-o} + \frac{G^*_{io-o}T^*_{ji-o}}{Z_L+Z^*_{o-o}})\cdot\hat{u}_{in} + \frac{Z_L T^*_{ji-o}}{Z_L+Z^*_{o-o}}\cdot\hat{j}_o + (G^*_{ci} + \frac{G^*_{co}T^*_{ji-o}}{Z_L+Z^*_{o-o}})\cdot\hat{c} \tag{3}$$

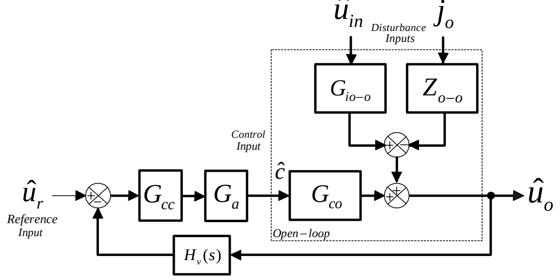

Fig. 3 Control-block diagram for closed-loop output dynamics.

The dynamical behaviour of a converter can be concluded according to the frequency response of its voltage-control loop gain $L(s)$, which can be defined to be as shown in (4) according to Fig. 3.

$$L(s) = H_v G_{cc} G_{ca} G_{co} \tag{4}$$

If the unterminated loop gain is denoted by $L^*(s)$, then the load-affected loop gain can be given as shown in (5) according to (2) due to changes in G_{co}.

$$L(s) = \frac{L^*(s)}{1+\dfrac{Z^*_{o-o}}{Z_L}} \tag{5}$$

The equation (5) explicitly defines that the impedance-type interactions would be reflected via the unterminated open-loop output impedance into the dynamics of the converter. If the open-loop output impedance is zero, the converter would be totally insensitive to load interactions but in practice such a condition is impossible to be accomplished [15]. The impedance ratio Z^*_{o-o}/Z_L in (5) is a similar minor-loop gain as defined in [16], and consequently, the stability and performance of the converter cannot be concluded by using it only.

The same equation as (5) has been derived in [5]-[7] but the open-loop output impedance is replaced by its equivalent $(1+L^*(s))Z^*_{o-c}$. The discussions following the derivation have been, however, conducted by using the closed-loop output impedance Z^*_{o-c} as if the term $(1+L^*(s))$ were obsolete. Therefore, there are visible conflicts between the discussions and the figures demonstrating the load effects especially in [6],[7].

According to the control theory [13], we may derive internal stability conditions for the system comprising of the closed-loop converter and load (Fig. 2) specifying four transfer functions of which one is $1/(1+Z^*_{o-c}/Z_L)$. In the case of minimum-phase system, it is sufficient to consider the stability of one of those transfer functions. In this case, the closed-loop impedance ratio Z^*_{o-c}/Z_L is the main loop gain, and therefore, the *Nyquist* stability criteria can be applied. The robust performance (i.e., gain and phase margins) associated to this impedance ratio does not necessarily comply with the robust performance of the converter.

It may be observed that Z^*_{o-c}/Z_L has inverse relation to the loop gain of the associated converter at those frequencies, where the magnitude of the loop gain is high. Close to the end of the control bandwidth the relation is weak. We do not go any further with the theoretical discussions but the results will be published in due time.

According to (3), the impedance-type load affects also the input parameters, and may cause increase in the sensitivity to the input-side interactions [11],[16], which should be also carefully studied.

3 Experimental Load-Interaction Analysis

The load interactions are experimentally verified by using the voltage-mode-controlled (VMC) buck converter shown in Fig. 4. The converter load was a *LC*-filtered resistor of 4 Ω. The resonant frequency of the *LC* filter was varied. The experimental frequency-response measurements were carried out by using Venable Industries' frequency-response analyzer Model 3120 with an impedance-measurement set. The measured data were converted into Matlab™ data form for efficient figure handling. All the figures in this section show experimental measurements.

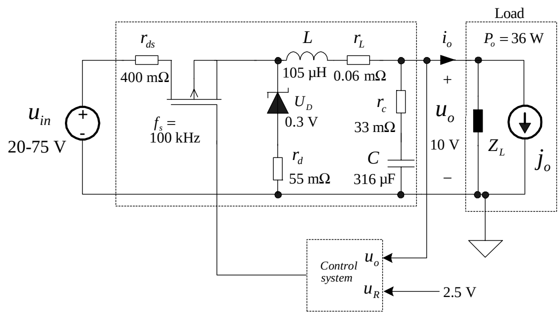

Fig. 4 Experimental VMC buck converter

The open-loop (Z^*_{o-o}) and closed-loop (Z^*_{o-c}) output impedances of the converter at the input voltage of 50 V as well as the load impedances, when the load-resonant frequency was close to the resonant frequency of the converter (i.e., ≈ 1 kHz) are shown in Fig. 5.

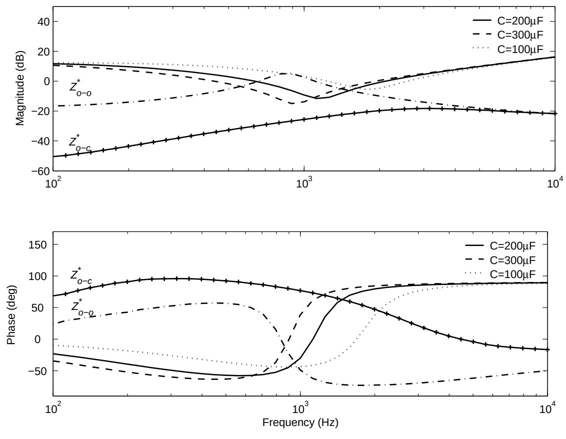

Fig. 5 The open (Z^*_{o-o}) and closed-loop (Z^*_{o-c}) output as well as the load impedances having resonant frequency close to the converter resonant frequency.

The load impedances denoted using solid and dashed lines are substantially less than the open-loop output impedance depicting strong effect on the loop gain. The control bandwidth would not be affected, because the load impedances are still higher than the closed-loop output impedance. The load impedance denoted by using dotted line would not affect much the loop gain, because it is higher than the open-loop output impedance. The corresponding load-affected loop gains are shown in Fig. 6 confirming the above analysis made according to Fig. 5.

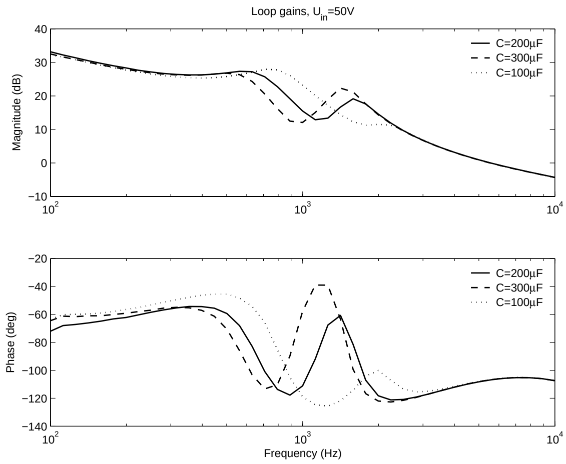

Fig. 6 The load-affected loop gains at the input voltage of 50 V with the impedance-type loads shown in Fig. 5.

The resonant frequency of the *LC*-filtered load was tuned close to the control bandwidth of the original converter (≈ 5 kHz). The corresponding load impedances and the open (dash-dot line) and closed-loop (line with '+' – sign) output impedances are shown in Fig. 7.

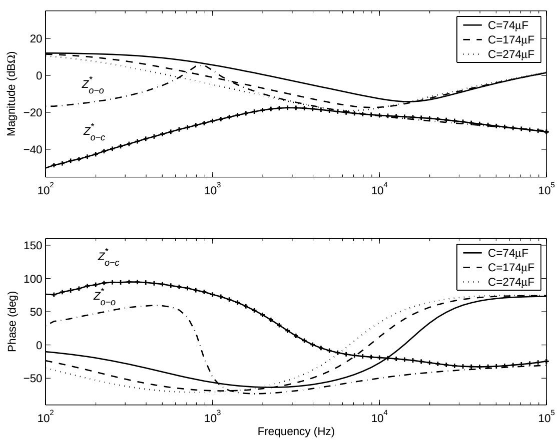

Fig. 7 Open (Z^*_{o-o}) and closed-loop (Z^*_{o-c}) output as well as the load impedances having resonant frequency close to the end of the control bandwidth.

If the load-interaction analysis would be based on the closed-loop output impedance as suggested in [5]-[7], the expected effect on the loop gain would be small. The corresponding load-affected loop gains are shown in Fig. 8 depicting, however, reduced control bandwidths with slightly improved phase margins, which may be predicted using (5) and the shown open-loop output impedance.

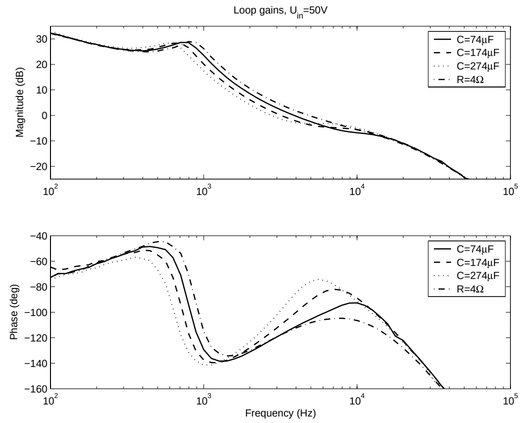

Fig. 8 Load-affected loop gains

The experimental measurements confirm definitively that the open-loop internal output impedance would be the element in a converter, which can be used to accurately predict the load interactions. It may be obvious according to the phase of the open-loop output impedance, Figs. 5 and 7, that the VMC buck converter is sensitive to a capacitive load at the frequencies less than the resonant frequency of the converter because of the inductive phase behaviour. At the frequencies higher than the converter resonant frequency, the phase margin tends to increase because of the capacitive phase of the open-loop output impedance. Different converters have different kind of load interactions depending on their open-loop output impedance. The interactions cannot be generalized.

4 Design of Load Invariance

It is obvious according to (2) that the output dynamics of a converter would stay intact if the open-loop internal output impedance is zero. The load will always affect the input dynamics (3), and may therefore, affect the overall dynamics of the converter despite the actions taken to reduce the open-loop output impedance. It was demonstrated in midd 1980's that the load-current feedback can improve the transient response of a peak-current-mode-controlled (PCMC) buck converter [17]. The conditions for obtaining zero output impedance were derived in early 1990 [18] stating that their general implementation is possible.

The conditions for zero output impedance [15] can be derived by using the control-block diagram shown in Fig. 9, where R_{s2} is the output-current-sensing resistor, H_i, the output-current-feedback gain and G_a the gain between the control voltage and duty ratio. According to Fig. 9, we can compute the affected output dynamics to be as shown in (6).

$$\begin{aligned} G^*_{co-ocf} &= G_a G^*_{co} \\ Z^*_{o-o-ocf} &= Z^*_{o-o} - R_{s2} H_i G_a G^*_{co} \\ G^*_{io-o-ocf} &= G^*_{io-o} \end{aligned} \tag{6}$$

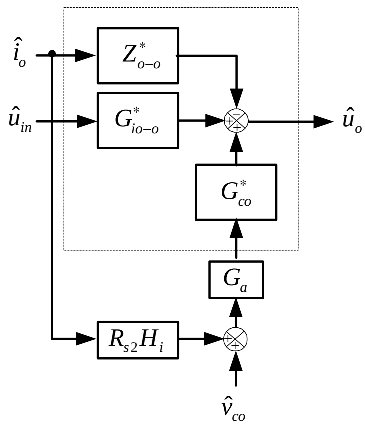

Fig. 9 Unterminated control-block diagram for output dynamics using load-current feedback.

According to (6), the zero-output-impedance conditions can be derived to be as shown in (7). The conditions stated in [18] may be the same but difficult to verify due to the method used. It is obvious that the zero-impedance conditions cannot be accomplished in the converters exhibiting non-minimum-phase behaviour (i.e., boost and buck-boost) due to the required unstable pole. It may be also obvious that a perfect zero output impedance cannot be accomplished in practice due to the parameter uncertainties and control delays [15].

$$H_i(s) = \frac{1}{R_{s2} G_a} \cdot \frac{Z^*_{o-o}}{G^*_{co}} \tag{7}$$

In a PCMC buck converter, the close-to-zero-output-impedance state can be obtained by using unity-output-current feedback (i.e., $H_i = 1$)[15],[17] and choosing the inductor- and output-current-sensing resistors to be equal. In an ideal case, the maximum output impedance is the equivalent series resistances of the inductor branch and the output capacitor, respectively, as shown in Fig. 10 [15]. The mismatch in the sensing resistor would gradually increase the output impedance and consequently, the load sensitivity. A more detailed analysis of the load invariance can be found from [15].

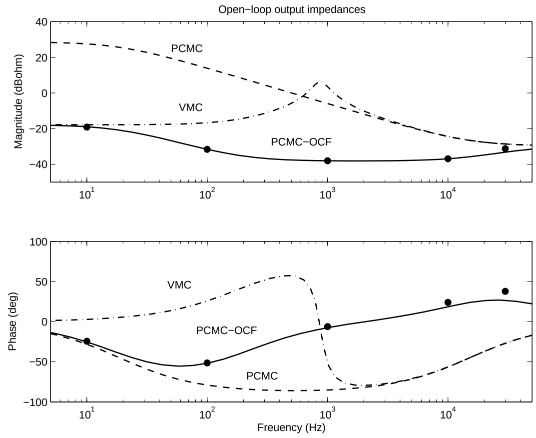

Fig. 10 Open-loop output impedances of VMC, PCMC and PCMC-OCF (i.e., output current feedback) buck converters using the same power stage as in Fig. 4 [15]. The dot marks denote the frequency responses derived from the simulation model by using FFT.

5 Conclusions

The load interactions in a regulated converter were studied. It has been claimed that the interactions can be eliminated by designing the closed-loop internal output impedance to be small. It was shown, however, theoretically and experimentally that the load interactions are reflected into the converter dynamics via the open-loop output impedance. Therefore, the loop gain will always be affected, whenever the load impedance is less or close to the open-loop output impedance. At those frequencies, where the loop gain is high, the closed-loop output impedance acts as a boundary for the loop gain reduction. The converter would be most sensitive to load effects taking place at the vicinity of the end of control bandwidth, respectively. As a consequence, the only viable method to reduce the load sensitivity is to design the open-loop output impedance to be small.

6 Literature

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